N tic of Allowability	Application No.	Applicant(s)	
	10/726,518	PARK ET AL.	
	Examiner	Art Unit	
	Sameer K. Gokhale	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/22/05*.

2. ☒ The allowed claim(s) is/are *1-39*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☒ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: *KR 2002-76723*.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 4-22-05, 12-4-03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in on December 4, 2003. It is noted, however, that applicant has not filed a certified copy of the Korea 2002-76723 application as required by 35 U.S.C. 119(b).

Allowable Subject Matter

2. Claims 1-39 are allowed.

The following is an examiner's statement of reasons for allowance:

3. Relative to independent claims 1 and 21, Tanaka et al. (US 5,798,744, hereafter "Tanaka") teaches a system and method comprising: gate and data lines crossing each other (Fig. 4); a pixel thin film transistor (Fig. 18, TFT) including gate, source and drain electrodes (Fig. 18), the gate electrode connected to the gate line and the source electrode connected to the data line (Fig. 18); a liquid crystal capacitor (Fig. 18, CLC) connected to the drain electrode of the pixel thin film transistor (Fig. 18); a first switch thin film transistor connected to a first end of the data line (Fig. 4, 301); a voltage source (Fig. 4, Vdd1) connected to a source electrode of the first switch thin film transistor.

Takabatake et al. (US 5,430,460, hereafter "Takabatake") teaches a system and method comprising a voltage source electrically connected to the drain electrode of the pixel thin film transistor (Fig. 4A, where the voltage across the top scanning line VGK-1 is a voltage source electrically connected to the drain electrode of the pixel TFT of line VGK).

Sasaki (US 6,100,865) teaches a system and method comprising a second switch thin film transistor (Fig. 1, 104) connected to a first end of the gate line (Fig. 1) and a voltage source connected to a source electrode of the second switch thin film transistor (Fig. 1, Vcc).

However, the primary difference between the teaching of the prior art of record (Tanaka, Takabatake, and Sasaki) and the instant invention is that said prior art does not teach a single voltage source connected to gate electrodes of both the first and second switch thin film transistors.

4. Relative to independent claims 10 and 26, Tanaka teaches a system and method comprising: gate and data lines crossing each other (Fig. 4); a pixel thin film transistor (Fig. 18, TFT) including gate, source and drain electrodes (Fig. 18), the gate electrode connected to the gate line and the source electrode connected to the data line (Fig. 18); a liquid crystal capacitor (Fig. 18, CLC) connected to the drain electrode of the pixel thin film transistor (Fig. 18); a multiplexing thin film transistor connected to a second end of the data line (Fig. 4, 301); a gate driver integrated circuit (IC) connected to a second end of the gate line (Fig. 4, 21); and a data driver integrated circuit (IC) connected to the multiplexing thin film transistor (Fig. 4, 21, where it would have been obvious that the gate driver can be separate from the data driver), wherein the data driver IC includes a data driver voltage source(Fig. 4, Vdd1) and a multiplexing circuit signal source (Fig. 4, CL1) such that the data driver voltage source is connected to a source electrode of the

multiplexing thin film transistor and the multiplexing circuit signal source is connected to a gate electrode of the multiplexing thin film transistor (Fig. 4).

Takabatake teaches a system and method comprising a voltage source electrically connected to the drain electrode of the pixel thin film transistor (Fig. 4A, where the voltage across the top scanning line VGK-1 is a voltage source electrically connected to the drain electrode of the pixel TFT of line VGK).

Sasaki teaches a system and method comprising a second switch thin film transistor (Fig. 1, 104) connected to a first end of the gate line (Fig. 1); a voltage source connected to a source electrode of the second switch thin film transistor (Fig. 1, Vcc); and a voltage source connected to the gate electrode of the second switch thin film transistor (see Fig. 1, ine G1).

However, the primary difference between the teaching of the prior art of record (Tanaka, Takabatake, and Sasaki) and the instant invention is that said prior art does not teach a separate first switch thin film transistor connected to a first end of the data line (this differs from claim 1 because in claim 1, the multiplexing thin film transistor was used as the first switch thin film transistor, but here it is already claimed separately), subsequently the said prior art does not teach a second voltage source connected to a source electrode of the first switch thin film transistor or a third voltage source connected to a gate electrode of the first switch thin film transistor.

5. Relative to independent claims 15 and 33, Tanaka teaches a system and method comprising: gate and data lines crossing each other (Fig. 4); a pixel thin film transistor

(Fig. 18, TFT) including gate, source and drain electrodes (Fig. 18), the gate electrode connected to the gate line and the source electrode connected to the data line (Fig. 18); a liquid crystal capacitor (Fig. 18, CLC) connected to the drain electrode of the pixel thin film transistor (Fig. 18); a multiplexing thin film transistor connected to a second end of the data line (Fig. 4, 301); and a data driver integrated circuit (IC) connected to the multiplexing thin film transistor (Fig. 4, 21, where it would have been obvious that the gate driver can be separate from the data driver), wherein the data driver IC includes a data driver voltage source(Fig. 4, Vdd1) and a multiplexing circuit signal source (Fig. 4, CL1) such that the data driver voltage source is connected to a source electrode of the multiplexing thin film transistor and the multiplexing circuit signal source is connected to a gate electrode of the multiplexing thin film transistor (Fig. 4).

Takabatake teaches a system and method comprising a voltage source electrically connected to the drain electrode of the pixel thin film transistor (Fig. 4A, where the voltage across the top scanning line VGK-1 is a voltage source electrically connected to the drain electrode of the pixel TFT of line VGK).

Sasaki teaches a system and method comprising a switch thin film transistor (Fig. 1, 104) connected to a first end of the gate line (Fig. 1); a voltage source connected to a source electrode of the switch thin film transistor (Fig. 1, Vcc); and a voltage source connected to the gate electrode of the switch thin film transistor (see Fig. 1, ine G1).

However, the primary difference between the teaching of the prior art of record and the instant invention is that said prior art does not teach a first gate driver integrated circuit (IC) connected to the source electrode of the switch thin film transistor.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shimada et al. (US 5,506,598) teaches a method for reducing the OFF-current in pixel TFTs. Koyama et al. (US 5,764,321) teaches a method for reducing the OFF-current in pixel TFTs based on the voltage between the source and the drain of the TFT. Yamazaki et al. (US 5,349,366) teaches a pixel TFT with a voltage source connected to the drain of the TFT. Lee (US 6,317,109) teaches a method of reducing residual images in a display. Kim et al. (US 7,038,644) teaches a method of applying an OFF-stress to a display.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sameer K. Gokhale whose telephone number is (571) 272-5553. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SKG
June 9, 2006

Sameer Gokhale
Examiner
Art Unit 2629

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600